WHAT IS CLAIMED IS:

1. A switching system for interconnecting plural kinds of communication networks and transferring information among the networks, comprising:

plural kinds of interfaces for converting signals from the plural kinds of communication networks into asynchronous transfer mode cells (ATM cells);

an ATM switch having pluralities of input and output
10 lines for transferring an ATM cell received by any one of the input lines from one of the interfaces to any one of the output lines based on header information of the ATM cell; and

plural kinds of signal processors, each of which
15 converts control information outputted from one of the interfaces into a signal format, alternatively a protocol, used by each of the plural kinds of communication networks.

2. A switching system according to claim 1, further
20 comprising a control processor connected to the ATM switch for inputting/outputting an ATM cell containing the control information with any one of the plural kinds of interfaces, alternatively of the plural kinds of signal processors, and executing necessary one of plural kinds of processing
25 operations.

3. A switching system according to claim 2, wherein said control processor includes plural kinds of processors for executing different processing, and a second ATM switch
30 connected to one of the plural kinds of processors for transferring inter-processor information to the other processor as a destination based on header information of

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an ATM cell,

said processor outputs an ATM cell having a header destined to the other processor performing necessary control to the second ATM switch, and said second ATM

5 switch transmits the ATM cell to the other processor as a destination.

4. A switching system according to claim 1, wherein each of said signal processors forms an ATM cell having a header

10 destined to any one of the processors, alternatively the interfaces, and outputs the ATM cell.

5. A switching system according to claim 1, wherein each of said signal processors relays an IP packet converted into

15 an ATM cell among the plural kinds of communication networks.

6. A switching system according to claim 1, wherein each of said signal processors converts the ATM cell based on a

20 signal received through a common line, and then outputs the cell to one of the communication networks.

7. A switching system according to claim 1, wherein each of said signal processors is provided in each of the

25 interfaces.

8. A switching system according to claim 1, wherein each of said interfaces converts control information received from one of the communication networks into an ATM cell having a

30 header destined to any one of the signal processors for performing signal processing, and outputs the ATM cell to the ATM switch.

9. A switching control method for interconnecting a plurality of communication networks and transferring information, comprising the steps of:

5   when call origination is made from a first communication network to a different second communication network, causing one of a plurality of interfaces having received a control signal to convert the control signal into a format of a first ATM cell having a header information destined to one of a plurality of signal
10 processors for performing signal processing, and then output the first ATM cell;

causing an ATM switch to transfer the first ATM cell to a specified and selected signal processor based on the
15 header information;

causing the selected signal processor to perform conversion for the received first ATM cell by a specified signal format, alternatively a specified protocol, and form a second ATM cell having a header information destined to a
20 first control processor, alternatively an interface connected to the second communication network, for processing the control signal and then output the same; and

causing the ATM switch to transfer the second ATM cell to the selected one of the first control processor,
25 alternatively one of the interfaces connected to the second communication network.

10. A switching control method according to claim 9, wherein by said ATM switch, an ATM cell is switched,
30 converted and then transmitted/received between a first interface connected to the first communication network and a second interface connected to the second communication

network.

11. A switching control method according to claim 9, wherein by a control processor connected to the ATM switch, an ATM cell containing control information is inputted/outputted with any one of the plural kinds of interfaces, alternatively the plural kinds of signal processors, and necessary one among plural kinds of processing operations is executed.

12. A switching control method according to claim 11, wherein said control processor causes one of plural kinds of processors executing processing operations different from each other to output an ATM cell to a second ATM switch, the ATM cell having a header destined to the other processor for performing necessary control, and said second ATM switch is connected to the plural kinds of processors, and transfers inter-processor control information to the other processor as a destination of the ATM cell based on the header information of the ATM cell.

13. A switching control method according to claim 9, wherein each of said signal processors forms an ATM cell having a header destined to any one of the processors for processing a control signal, alternatively the interfaces, and then outputs the same.

14. A switching control method according to claim 9, wherein each of said signal processors relays an IP packet converted into an ATM cell among the plural kinds of communication networks.

15. A switching control method according to claim 9, wherein each of said signal processors converts the ATM cell based on a signal received through a common line, and then outputs the cell to one of the communication networks.

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16. A switching control method according to claim 9, wherein each of said signal processors is provided in each of the interfaces.

10   17. A switching control method according to claim 9, wherein each of said interfaces converts control information received from one of the communication networks into an ATM cell having a header destined to any one of the signal processors for performing signal processing, and
15   then outputs the ATM cell to the ATM switch.